ABSTRACT OF THE DISCLOSURE

An array of memory cells configured to store at least one bit per one F^2 includes substantially vertical structures providing an electronic memory function spaced apart a distance equal to one half of a minimum pitch of the array. The structures providing the electronic memory function are configured to store more than one bit per gate. The array also includes electrical contacts to the memory cells including the substantially vertical structures. The cells can be programmed to have one of a number of charge levels trapped in the gate insulator adjacent to the first source/drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) and such that the programmed cell operates at reduced drain source current.